Coupled Electrical and Thermal 3D IC Centric Microfluidic Heat Sink Design and Technology

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Abstract

Through-silicon via (TSV) technology, an enabler for 3D ICs, has evolved, enabling thinner and shorter TSVs within substantially thinned wafers to achieve faster interconnects, large bandwidth density, and low power consumption. Yet, heat dissipation in 3D ICs becomes more and more challenging, especially in applications that require stacking of multiple processor and memory chips. Microfluidic cooling has been proposed as a solution to reject heat from 3D stacks that contain processor chips. However, current liquid cooling technology inevitably increases the wafer thickness, which is contrary to TSV technology trend. To date, little work has been done to optimize heat sink design to benefit TSV performance, and no attempt has been made to analyze the corresponding impact of a particular heat sink design on the performance of the electrical TSVs. A heat sink design without consideration of TSV performance can greatly diminish the advantages of 3D ICs. This paper presents a holistic cooling solution for 3D ICs, which not only meets thermal requirements, but also minimizes TSV parasitics that impact latency, bandwidth density, and power consumption. This paper will report: a) the design of a 3D-centric heat sink, b) the fabrication of the heat sink and associated high aspect ratio integrated TSVs, c) the thermal testing of the liquid-cooled heat sink and comparison to air-cooled heat sink, and d) the impact of the heat sink geometry on TSV capacitance.

Keywords

3D IC; microchannel heat sink; micropin-fin heat sink; through-silicon via (TSV); Electrical model of TSV

I. Introduction

The scaling of transistors in integrated circuits (ICs) has propelled the semiconductor industry during the past 50 years as it leads to improvements in system performance, power dissipation, and cost [1]. However, as the operating frequency has historically spiraled upwards and the number of cores increases on a chip, interconnect scaling has become a key performance-limiting factor [2]. This is true for both on-chip as well as off-chip interconnects. In the latter, the inability to have high density off-chip wires with low latency, low energy-per-bit and large bandwidth density has greatly exacerbated the memory wall problem for multicore processors. This is critical because off-chip bandwidth between multiprocessors and DRAM critically impacts system performance as measured in instructions per cycle (or seconds). To overcome this limit and continue the performance gains from scaling, implementation of 3D IC technology is being pursued by many. Three-dimensional stacked ICs represent a promising solution to the interconnect problem by significantly shortening the interconnect length as well as enabling the heterogeneous integration of logic, memory, MEMS systems, and optoelectronic devices [3][4]. However, the power density is much higher for 3D ICs for a given area. In high power applications, thermal management becomes a key problem. Previous work has shown the possibility of using liquid cooling instead of conventional air-cooling in 3D systems [5][6][7][8]. In addition to the thermal management issue, TSV technology development is another significant issue for 3D ICs. TSV technology is an enabling technology for 3D ICs as it provides the intra-layer communication such as communication between stacked processor and memory chips. Thinner and shorter TSVs result in faster interconnects, larger bandwidth density, and lower power consumption. But, to date, there has been neither an attempt to optimize the heat sink design while accounting TSV performance nor an attempt to analyze the corresponding impact of the microfluidic heat sink on the performance of the electrical TSVs.

This paper discusses the trade-offs between thermal resistance and pressure drop for different heat sink designs while also accounting TSV electrical performance. The heat removal capability of a liquid-cooled pin-fin heat sink and an air-cooled heat sink are compared. A staggered pin-fin heat sink is shown to be able to provide a thermal resistance as low as 0.27 K*cm^2/W with a flow rate of 70 mL/min for a heat sink depth of 200μm. The air-cooled heat sink possesses a thermal resistance of 0.518 K*cm^2/W for an air flow rate of 54.8 CFM. The heat sink's impact on electrical TSVs is discussed; analysis shows that the heat sink needs to be as thin as possible to benefit TSV fabrication, and high aspect ratio TSVs are preferred in signaling. Finally, novel methods to integrate the microfluidic layer with CMOS are described.

II. Circular Pin-fin heat sink and heat removal analysis

A. Basic Heat Transfer Theory

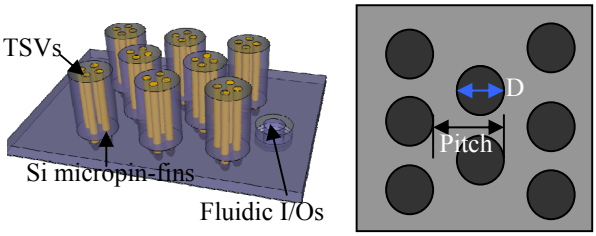

Figure 1: Staggered micropin-fin heat sink concept.

Microfluidic heat sink integration in a silicon substrate has been widely investigated during the past decades. Due to its relative ease of fabrication, the microchannel heat sink is popular among researchers. However, as microfabrication

technology advances, more complex cooling methods can be achieved, which brings the possibility to outshine the microchannel heat sink [9]. One method to enhance single-phase cooling utilizes the fabrication of obstructions in the flow direction. In this work, we explore the design of a staggered circular pin-fin structure (Figure 1) and its impact on 3D ICs (specifically, the electrical TSVs). Thermal resistance is one of the key parameters to evaluate a heat sink. In theory, the total thermal resistance (R_{tot}) consists of three parts: R_{cond} is due to the conductance from the circuit through the substrate and heat sink interface; R_{conv} accounts for the convection from the substrate to the liquid; R_{heat} is due to the increase of the fluidic temperature as it goes further into the heat sink [10]. In most cases, R_{cond} has a small contribution since the heat sink is very near to the heat source and can be neglected. In theory, R_{tot} is derived as follows:

$$R_{tot} = R_{conv} + R_{heat} \tag{1}$$

$$R_{tot} = \frac{1}{h_{ave} A_t} + \frac{1}{W_t c_p} \tag{2}$$

where W_t, and c_p are mass flow rate and specific heat capacity, respectively. The heat transfer coefficient, h_{ave}, is given by

$$h_{ave} = \frac{Nuk_f}{D} \tag{3}$$

$$Nu = C \,\mathrm{Re}^m \,\mathrm{Pr}^{0.36} \left(\frac{\mathrm{Pr}}{\mathrm{Pr}_s}\right)^{0.25} \tag{4}$$

where k_f and D are the thermal conductivity of the fluid and the diameter of a single fin. The Nusselt number, Nu, can be evaluated using the Eq.(4) [11] where Re and Pr are the the Reynolds number and Prandtl number evaluated using the bulk fluid properties and Pr_s is the Prandtl number using the fluid property at the surface temperature. This model is valid for certain conditions: $10 < \mathrm{Re} < 1000$, $200\mu m < H_{fin} < 400\mu m$, $20 < L/H_{fin} < 200$ with a pitch to diameter ratio of 1.25 and 3 [9]. A_t is the effective heat transfer area described as follows;

$$A_t = A_b + \eta A_{fin} \tag{5}$$

$$\eta = \frac{\tanh\left(2H_{fin}\sqrt{h_{ave}/k_{si}D}\right)}{2H_{fin}\sqrt{h_{ave}/k_{si}D}} \tag{6}$$

where k_{si}, H_{fin}, and η are the thermal conductivity of silicon, fin height and fin efficiency, respectively. A_b is the base area exposed to fluid, and A_{fin} is the total surface area of the pin-fins.

$$A_b = A_{tot} - \frac{1}{4} n \pi D^2 \tag{7}$$

$$A_{fin} = n\left(\pi D H_{fin} + \frac{\pi D^2}{4}\right) \approx n \pi D H_{fin} \tag{8}$$

$$n = \frac{(W - W_s)(L - L_s)}{P_w P_l} \tag{9}$$

where W, L are the width and length of the entire chip; W_s ,L_s, P_w, P_l are the horizontal and vertical spacing and the pitch between pins. n is the total number of pins.

B. Design Considerations

With the guidance of the model, the variables H_{fin}, D, and the pitch-to-diameter ratio need to be optimized for the maximum heat removal capability. From a standpoint of thermal performance, high pitch-to-diameter ratio gives larger flow path and thus smaller pressure drop but less heat transfer coefficient. Higher H_{fin} normally means higher effective heat transfer area until the decrease of η causes negative effects. Since higher H_{fin} provides larger flow path, reduced pressure drop across the heat sink is the result at higher H_{fin}. [12][13]. The optimal heat sink design from a thermal point of view (obtaining the minimal thermal resistance at a given pressure) is a complex topic. Many have derived optimal heat sink structures for either microchannel or inline/staggered micropin-fin heat sinks; some results are summarized in Table 1 [12][14].

Table 1: Selected optimal heat sink dimensions from literature.

Heat Sink Type	Dimensions (μm)
Microchannel [14]	Channel width (w_c) = 65 Wall width (w_w) = 24 Channel height(H_{ch}) = 399.75
Microchannel [12]	w_c = 65 w_w = 63.7 H_{ch} = 929.5
Staggered micropin-fin [12]	D = 196 $Pitch$ = 305.8 H_{fin} = 3155

However, in 3D IC applications, our focus is not only the best heat removal capability, but we also have to keep in mind the design that benefits the system performance, specifically the TSV technology. The most important factor is the height of the pin (H_{fin}). H_{fin} greatly impacts TSV diameter, TSV density and TSV capacitance which influences interconnect latency and power consumption. A high H_{fin} value, such as 900μm (Table 1), comes with a large TSV diameter and large latency which is not desirable in 3D ICs (even if the structure can be fabricated).

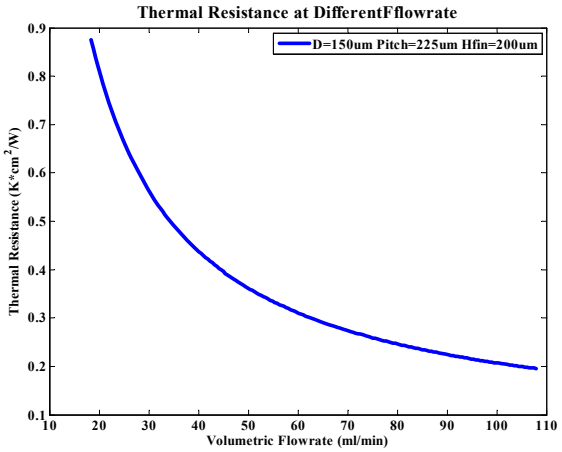

Figure 2: Thermal resistance as a function of volumetric flow rate.

Thus, H_{fin} should be as small as possible to achieve the best system performance. Yet, H_{fin} needs to be greater than a certain value (~150µm) in order to keep the pressure drop tolerable. Additional analysis of the heat sink geometry's impact on TSV characteristics is described later in the paper.

To obtain a thermal resistance of ~0.2 K·cm^2/W while maintaining a relatively small die thickness, we set the micropin-fin configuration to be: D = 150µm, $Pitch$ = 225µm, H_{fin} = 200µm. The modeled thermal resistance for such a configuration is plotted in Figure 2.

III. Fabrication Details of the Thermal Testbed

Figure 3 illustrates the necessary steps for the fabrication of a silicon chip with an integrated micropin-fin heat sink.

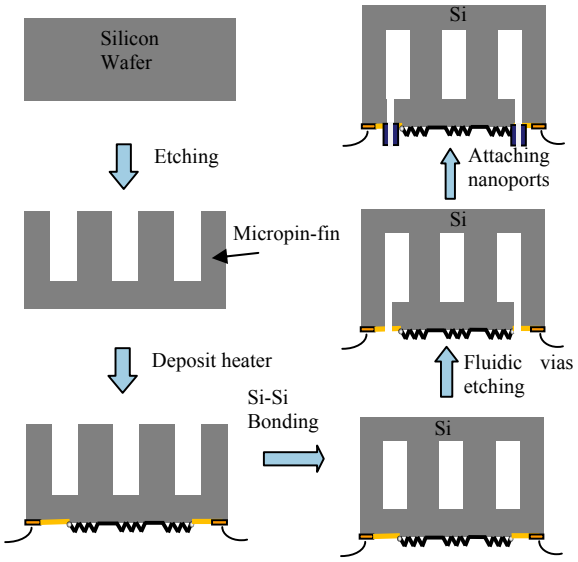

Figure 3: Process flow of micropin-fin heat sink.

The fabrication of the micropin-fin heat sink starts with a double-side polished silicon wafer. Using the standard bosch process, which alternates between an SF_6 plasma etch step and an inert C_4F_8 deposition step, the 200µm (±2µm) deep micropin-fin array is etched. The diameter of a single pin-fin is 150µm, and the pitch of the pin-fins is 225um. A localized SEM image of individual micropin-fins is shown in Figure 4(a). Figure 4(b) shows an overall view of the miciropin-fin heat sink. A platinum spiral heater is sputter-coated and patterned onto the back side of the wafer to simulate the heating of a microprocessor. Due to the extreme linear resistance-temperature relationship and its chemical inertness, the Pt heater also serves as the temperature sensor during the thermal measurements. The next step is to encapsulate the micropin-fins. Several bonding methods have been performed and tested by many in the literature [15][16]. Using an intermediate layer such as SU-8 requires a low bonding temperature (<200°C). The bonding quality is fairly independent of the surface roughness and planarity [15]. However, in order to prevent the degradation of SU-8, the bonded sample cannot be exposed to a temperature higher than ~380°C [17]. Furthermore, for 3D IC cooling applications, it is necessary to integrate the TSVs into the microfluidic heat sink layer. Therefore, a direct bonding method is preferred in 3D IC applications. In this paper, an oxygen plasma is used to activate the silicon surface and enables the bonding of two silicon wafers at room temperature. An anneal at 400°C increases the bonding strength by forming Si-O-Si bonds [16]. Figure 4(c) is an infrared image of the top view of the bonded wafer from which we can see the bonding yield is high. Air and metal appear brighter than the silicon surface in the IR image. We can see that there is no air trapped between the top of the pin-fins and the capping wafer (the brighter color is the underlying Pt heater). Fluidic vias are then etched to enable liquid circulation into and out of the heat sink.

As will be shown later, the sample used for the air-cooled heat sink testing only contains the platinum heater/resistance thermal detector (RTD) features.

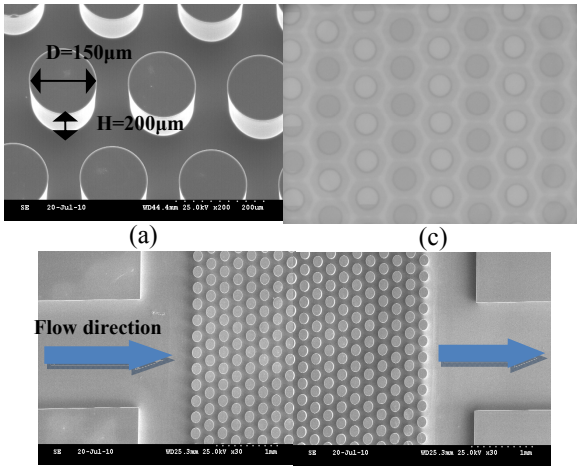

Figure 4: a) SEM image of individual pin-fins b) overall view of the heat sink c) infrared image of top view of encapsulated micropin-fin heat sink and the underlying platinum heater.

IV. Thermal Test Setup and Results for Air-Cooled Heat Sink and Microfluidic Heat Sink

This section discusses the thermal test setup and testing results for a) a single chip with an embedded micropin-fin heat sink and b) a single chip using air cooling. Figure 5 shows the typical structures of the air-cooled heat sink and the microfluidic heat sink. Figure 6 shows the test-beds for the air-cooled heat sink (ACHS) and the 3D IC centric ultra thin microfluidic heat sink (MFHS).

By placing the MFHS test-bed and the ACHS test-bed side-by-side, we can clearly see the volume difference of the two cooling technologies. For comparison, the dimensions of the MFHS are 0.6x0.6x0.02 cm while that of the ACHS are 13x10x6 cm. The volume of the two heat sinks differs by a factor of 10^5.

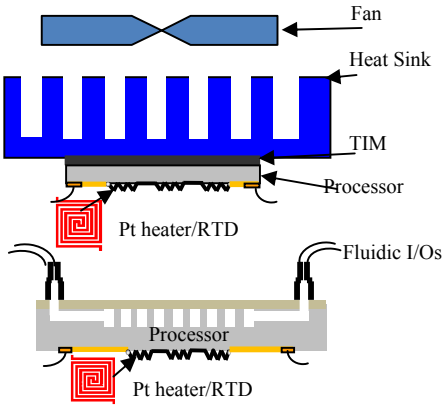

Figure 5: Thermal test setup for air-cooled heat sink (top) and microfluidic (bottom) heat sink.

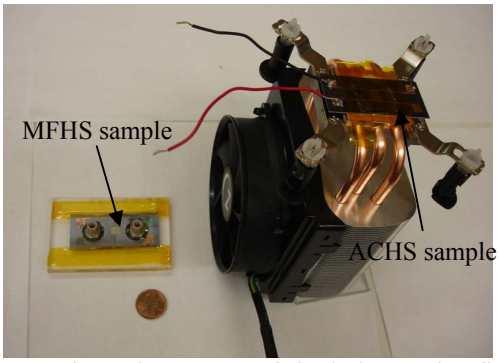

Figure 6: Thermal test setup of single-layer microfluidic heat sink (MFHS) and air-cooled heat sink (ACHS).

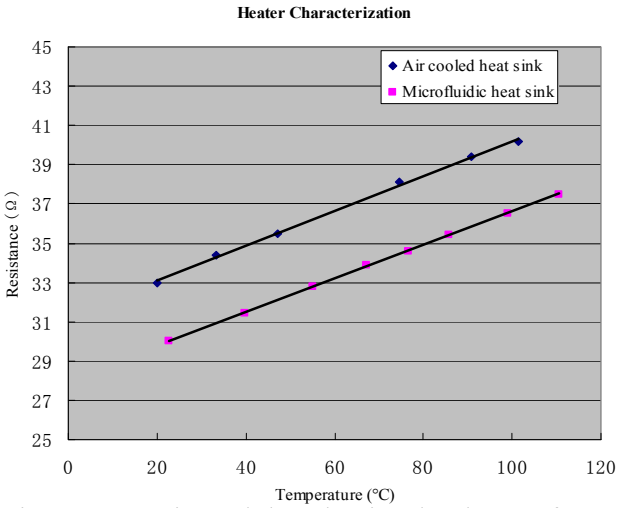

Figure 7: Experimental data showing the change of RTD resistance is a linear function of temperature.

The experiment starts with the characterization of the platinum heater/RTD. Figure 7 verifies that the resistance-temperature relationship of platinum is linear. The relationship between the resistance and the temperature is expressed in Eq. (10), where R(T) and R(T_0) are the resistance of the Pt RTD at T and T_0, α is the dimensionless temperature coefficient. Based on the slopes in Figure 7 and Eq.(10), the temperature coefficients of the heater on the ACHS sample and the MFHS sample are calculated to be 0.00267 and 0.002864. From various fabricated Pt heaters, α varies in the range of 0.0026-0.0029, which shows good consistency.

$$R(T) = R(T_0) + \alpha R(T_0)(T - T_0) \quad (10)$$

In the ACHS experiment, we use a commercially available CPU cooler which consists of 3 copper heat pipes and 45 aluminum fins that is designed for the Intel i5/i7 CPU. The ACHS sample is tested while the fan is rotating at its maximum speed (2500rpm $\pm 15\%$). The corresponding air flow is 54.8 CFM. For the MFHS testing, we used the sample with an embedded micropin-fin heat sink, which is fabricated as described in the previous section. The thermal measurements are made at two flow rates: 45 mL/min and 75 mL/min. The dissipated power density for both the ACHS and the MFHS goes up to ~100W/cm^2. The total heated area is 0.6 cm×0.6 cm.

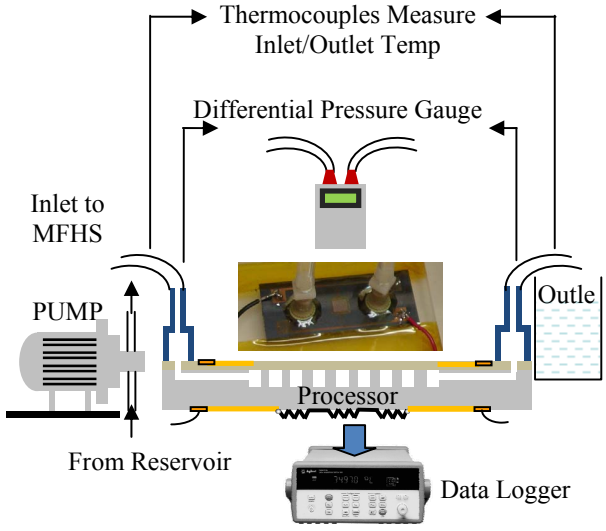

Figure 8: Schematic of the test setup for MFHS.

During the fluidic testing, DI water is pumped out of a tank by a gear pump and flows through the MFHS sample. The pressure gauge and T-type thermocouples are in parallel with the MFHS in order to measure the differential pressure drop across the heat sink and the inlet/outlet temperature of DI water. A data acquisition system is connected to the RTD and monitors the resistance every second (Figure 8). Experiments are done for air cooling and microfluidic cooling for different power densities, and the corresponding chip temperatures are plotted in Figure 9. The average junction temperature under the ACHS is 77.6 °C at 109 W/cm^2 for a flow rate of 54.8 CFM. In contrast, the average junction temperature under the MFHS cooling is 53.5 °C at 105 W/cm^2 for a flow rate of 45 mL/min and 47.9 °C at 103.4 W/cm^2 for a flow rate of 70 mL/min. We can see that at a certain power density, the chip under microfluidic cooling is cooler than the chip under air cooling. At lower operating temperature, the leakage current in CMOS circuits is smaller, which results in lower power consumption. Sekar et al. [18] has shown that by reducing the chip temperature from 88 °C to 47 °C, the total power of a high performance chip decreases from 102 W to 83 W.

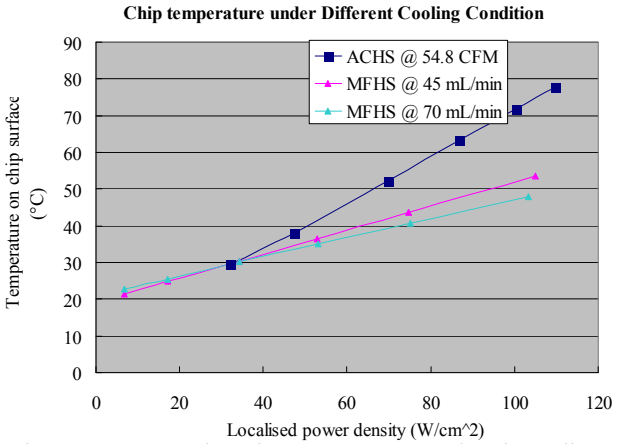

Figure 9: Average junction temperature under air cooling and microfluidic cooling.

The normalized thermal resistances of the ACHS and the MFHS under different flow rates are summarized in Table 2. The thermal resistances obtained from the compact physical modeling discussed earlier are listed for comparison as well. The difference in the calculated and measured values may be caused by the heat exchanging from the Pt heater to the surrounding air. Moreover, the heat generated from the heater also spreads from the heated area to the adjacent silicon. More experiments are needed to understand the spreading effect. The measured pressure drops are 38.5 kPa and 83 kPa for 45 mL/min and 70 mL/min, respectively. The measured pressure drops include the pressure drop across the micropin-fin array as well as the pressure drop over relatively long embedded leading microchannels.

Table 2. Comparison of the measured and modeled normalized thermal resistance for power density ~ 100W/cm^2.

	ACHS	MFHS @ 45 mL/min	MFHS @ 70 mL/min
Thermal Resistance (K·cm^2/W)	0.518	0.326	0.269
Localised power density (W/cm^2)	100.2	104.9	103.4
Modeled R_{TH} (K·cm^2/W)	-	0.3959	0.2735
Modeling Error	-	17.65%	1.7%

V. Heat Sink Architecture Impact on TSV Electrical Performance

A typical TSV structure is a hole in the silicon filled with a layer of thin oxide and copper. The empirical expression for TSV self-capacitance is as follows [19]:

The TSV oxide capacitance is given by:

$$C_{OX} = \frac{2\pi\varepsilon_{OX} L_{TSV}}{\ln(\frac{R_{via}}{R_{metal}})} \quad (11)$$

where ε_{OX} is the oxide permittivity, L_{TSV} is the TSV length, R_{via} and R_{metal} (Figure 10) are the radii of the via and copper.

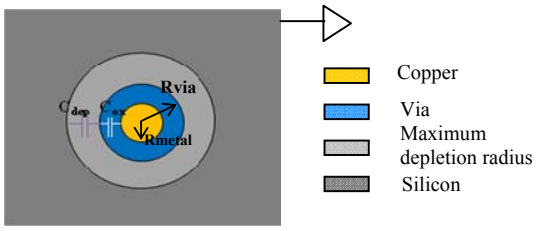

Figure 10: Top view of TSV in the silicon substrate [20].

When the voltage applied to TSVs is higher than the flat-band voltage ($V_{TSV} \geq V_{FB}$), the substrate is depleted so that the total capacitance is the series of the oxide capacitance and the depletion capacitance (C_{dep}) [20]. Specifically, when TSVs carry high frequency signals, the depletion radius reaches its maximum (R_{max}) when $V_{TSV} \geq V_{Th}$. Additionally, working at high frequency makes the inversion layer charge density unable to follow the fast variation in the gate voltage [19]. This maintains the depletion radius at R_{max}. Hence, the depletion capacitance reaches its minimum (C_{depmin}) (Figure 10):

$$C_{TSV\,\min} = \frac{C_{OX} C_{dep\,\min}}{C_{OX} + C_{dep\,\min}} \quad (12)$$

While

$$C_{dep\,\min} = \frac{2\pi\varepsilon_{si} L_{TSV}}{\ln(\frac{R_{\max}}{R_{via}})} \quad (13)$$

The C_{TSVmin} is modeled and plotted for different heat sink heights and different TSV aspect ratios, assuming the dielectric thickness is 100nm (Figure 11). Since the depletion capacitance also depends on the doping of the substrate, we use a typical doping level in the model.

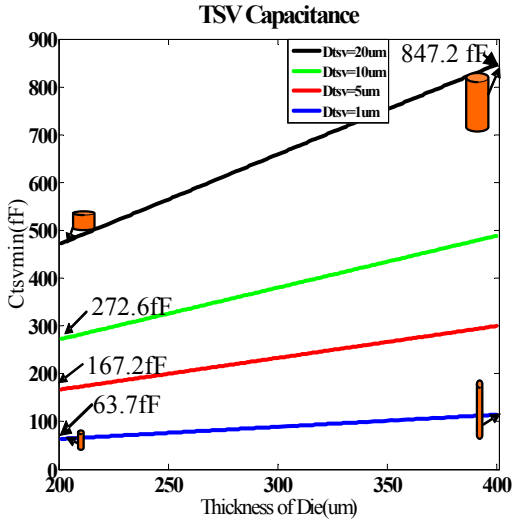

Figure 11: Minimum TSV capacitance as a function of the die thickness for different via diameter.

The TSV capacitance increases linearly with the thickness of the die. For example, assuming we are aspect ratio limited to 20:1, C_{TSV} for a 200µm micropin-fin design is 272.6 fF while that of a 400µm micropin-fin design, as optimized in Table 1, is 847.2 fF. If the TSV aspect ratio keeps increasing,

the TSV capacitance continuously decreases. Methods to decrease TSV capacitance will be discussed in Section VII. The capacitance reductions improve the interconnect latency and the power consumption, which raises the importance of another topic – the need for high aspect ratio TSVs.

As mentioned before, the heat sink architecture influences a number of critical aspects in the stack, including available silicon area for TSV placement, the number of TSVs, etc. Needless to say, we must have enough surface area, as dictated by 3D IC design, through the micropin-fins to route TSVs. In Figure 12, the available silicon surface decreases rapidly as the pitch to diameter ratio increases. For the micropin-fin heat sink design which is chosen in this paper, 34% of the silicon area is available for TSV routing.

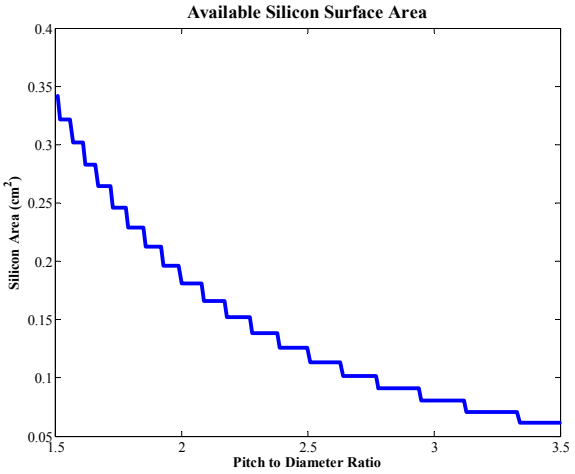

Figure 12: Available silicon area in the micropin-fin heat sink.

VI. High Aspect Ratio TSVs

A high aspect ratio TSV fabrication technology is developed to fit within the micropin-fin heat sink design and to improve TSV performance as discussed in the previous section. Figure 13 shows a local SEM image of a row of copper TSVs with an aspect ratio 20:1. Here, we demonstrate TSVs with a pitch of 15µm, which enables a density of 410,000 TSVs/cm^2. The height of the TSVs, which is 200 µm (Figure 13), was chosen to be compatible with the height of microfluidic heat sink under consideration.

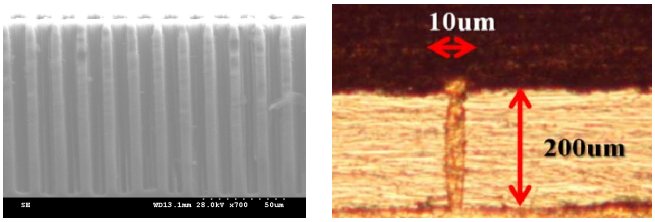

Figure 13: Cross-sectional SEM image (left) of a row of high density 10µm diameter TSVs and a cross-sectional optical image (right) of a single copper filled TSV.

VII. Alternative Ways to Reduce the TSV Capacitance

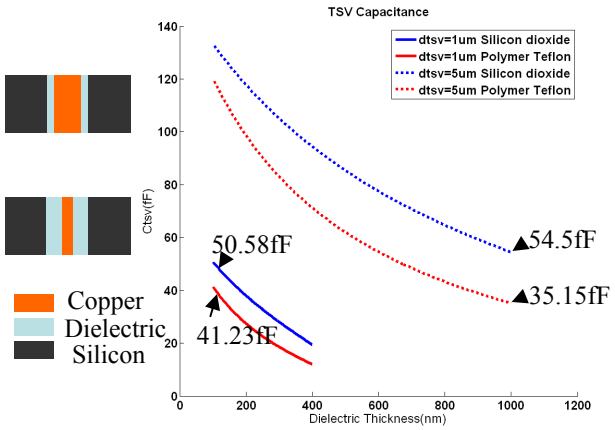

Figure 14: The minimum TSV capacitance using oxide and teflon as the dielectric.

Because of the integration of the micro-heat sink, the die thickness will be larger than ICs without a microfluidic heat sink. As a result, for a fixed aspect ratio, TSV diameter will increase leading to increasing TSV capacitance, which increases the interconnect latency and power consumption. We propose two solutions to compensate for the increased capacitance due to the larger diameter: a) increasing the oxide thickness; b) replacing the SiO_2 liner with polymer (or low-k value dielectric) (Figure 14). By increasing the dielectric thickness from 100nm to 1µm, the capacitance of a 5µm TSV becomes comparable with a 1µm TSV. The polymer dielectric also helps reduce the TSV capacitance by ~30% for 5µm TSVs.

VIII. Heterogeneous Integration

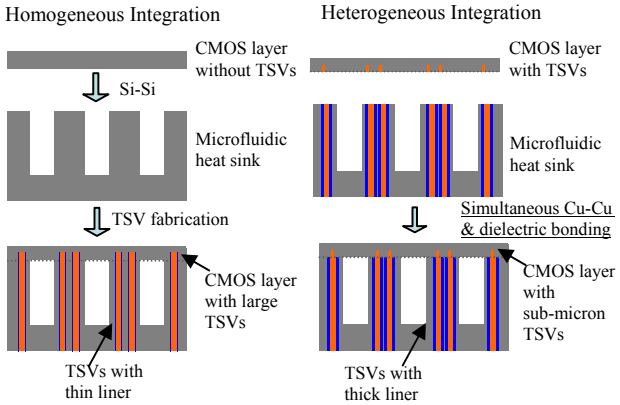

Figure 15: Homogeneous and heterogeneous approach to integrate the microfluidic layer with the CMOS layer.

There are two ways to integrate the microfluidic heat sink with CMOS (Figure 15) [21]. One method is the homogeneous approach. In this approach, the CMOS chip and microfluidic layer are fabricated without the TSVs. The two layers are then bonded, for example, using the Si-Si bonding technique discussed in the previous section. The last step involves etching of TSVs through this stack. The second approach is called heterogeneous integration. In this case, the

CMOS layer with the sub-microns TSVs and the microfluidic layer with larger TSVs are fabricated *independently*. The two layers are electrically and mechanically bonded using a hybrid bonding technique discussed in [22].

The advantages of heterogeneous bonding mainly involve three aspects. First, the TSVs in the CMOS layer become much smaller, leading to conservation of valuable silicon area in the CMOS chip. Table 3 illustrates how much area is saved by the heterogeneous bonding. Secondly, since the microfluidic layer is fabricated independently, the restrictions in temperature and material are eliminated. This creates more flexibility in processing for the microfluidic layer. Moreover, it enables one to pursue bottom-up plating for the TSVs in the liquid cooling layer, which can provide much higher aspect ratio TSVs. Finally, alternative ways to reduce the capacitance can be used in the microfluidic layer to make the total TSV capacitance as small as possible in order to improve the interconnect latency, energy consumption, etc.

Table 3. Comparison of the area occupied by TSVs for homogeneous and heterogeneous bonding.

	Assumption	Area occupied by TSVs in CMOS layer (cm2)
Homogeneous Integration	Chip area=1cm*1cm $H_{cooling}$=200um; H_{CMOS}=10um TSV aspect ratio=20:1 Number of TSVs=$0.5*10^5$	4.3%
Heterogeneous Integration		0.0098%

IX. CONCLUSION

The objective of the paper is to explore a holistic solution to address the thermal and electrical issues of 3D ICs. This paper first investigates microfluidic heat sink designs for 3D ICs. Interdisciplinary analysis has shown that the 3D centric ultra thin micropin-fin heat sink is potentially capable of cooling down the chip while being TSV compatible. In addition, microfluidic and air cooling are evaluated. From the experimental data, microfluidic cooling provides lower chip junction temperature with a much smaller heat sink volume compared to air cooling. Next, the impact of the heat sink geometry on the TSV capacitance is analyzed and shows the need for minimal H_{fin} and high aspect ratio TSVs. Finally, novel ideas are introduced to decrease TSV capacitance: a) thick dielectric liner and b) polymer clad TSVs. Methods to integrate the microfluidic heat sink layer with CMOS technology are also described.

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